UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/131,846	07/24/1998	DONALD EUGENE DENNING	TU9-98-010	8393

42640 7590 03/08/2005

DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HWY
SUITE 2110
AUSTIN, TX 78759

EXAMINER	
BONZO, BRYCE P	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/131,846	DENNING ET AL.	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s)_____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Official Action

Status of the Claims

Claims 1-18 are rejected under 35 USC §102.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Gates (United States Patent No. 5,701,409).

As per claim 1, Gates discloses:

specifying said hardware fault to simulate (column 2, lines 49-53: describes the loading of a command to deliberately cause a fault);

determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card (column 3, lines 38-46);

creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog voltage converter (column 3, lines 26-38; the digital-to-analog converter as described by Applicant is inherent to the PCI specification, and is described under the heading *Response to Amendments*); and

outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated (column 3, lines 26, 28)

As per claim 2, Gates discloses:

wherein said step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCU bus to simulate said hardware fault occurring on said expansion card (column 3, lines 26-28: the error be simulated is an incorrect parity).

As per claim 3, gates discloses:

further comprising the step of prior to outputting said analog voltage signal, determining a proper response of said system to said hardware fault (column 4, lines 12-18, 32-46, 54-64).

As per claim 4, Gates discloses:

further comprising the step of in response to outputting said analog voltage signal, determining if said system responded properly to said hardware fault (column 3, lines 15-22).

As per claim 5, Gates discloses:

further comprising the step of determining a line of said bus which is associated with said hardware fault (column 4, lines 58-64 and column 5, lines 8-62).

As per claim 6, Gates discloses:

further comprising the step of outputting said analog voltage signal during operation of said expansion card utilizing said line of said bus (column 4, lines 58-64).

As per claim 7, Gates discloses:

further comprising the step of determining a test voltage level for said analog voltage signal, wherein said test voltage level is is a voltage level required to simulate said fault (column 4, lines 58-64).

As per claim 8, Gates discloses:

further comprising the step of outing said analog voltage signal having said test voltage level during operation of said expansion card utilizing said line of said bus (column 4, lines 58-64).

As per claim 9, gates discloses:

wherein the step of determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card further comprises the step of determining a signal to output utilizing a PCI bus to simulate said hardware fault occurring on said expansion card (column 4, lines 58-64).

Claims 10-18 are directed to the data processing embodiment of the method for simulating a hardware fault of claim 10-18 are and rejected on the same grounds.

Response to Applicant's Arguments

First, Applicant has argued that Gates and PCI specification do not teach a digital-to-analog voltage converter. Applicant's specification as originally filed does not recite a digital-to-analog voltage converter, but does disclose digital-to-analog converter (DAC). The Examiner presumes these two devices to be the same element. Applicant's specification describes the function as "utilized to convert the digital information regarding the test voltage level to the proper analog voltage level." Applicant does not provide structural limitations for the device and as such the Examiner is relegated to using the functionality of the DAC as its defining characteristics. Gates clearly provides for this DAC functionality, taking a digital signal and conditioning it through analog manipulation for transport on the PCI bus with vary different physical requirements than that of the board from which the original digital signal was received.

Second, Applicant states "Applicants are not now claiming analog voltage versus digital voltage *per se*." In fact as those very words are explicitly recited, Applicant is claiming such a concept.

Applicant's timely filing of a Notice of Appeal is expected.

Final Disposition

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Primary Examiner
Art Unit 2114